REMARKS

Claims 1, 2, 4-12 and 38-64 are pending in the present application, were examined, and were rejected. In response, no claims are amended, no claims are added and no claims are cancelled. Applicants respectfully request reconsideration of pending Claims 1, 2, 4-12 and 38-64 and in view of at least the following remarks.

I. Claims Rejected Under 35 U.S.C. §103

The Patent Office rejects Claims 1-2, 4-12 and 38-64 under 35 U.S.C. §103(a) as being anticipated by U.S. Patent No. 5,778,431 to Rahman et al. ("Rahman") in view of U.S. Patent No. 5,524,433 to Milburn et al. ("Milburn"). Applicants respectfully traverse this rejection.

For the reasons provided below, the Examiner has failed to establish a *prima facie* case of obviousness in view of the references of record. Case law is quite clear in establishing that the combination of references cited by an Examiner must teach each and every feature of the claimed invention. The Federal Circuit Court of Appeals in In re Rijckaert, 9 F.3d 1531, 28 U.S.P.Q. 2d 1955 (Fed. Cir. 1993) held that:

> In rejecting claims under 35 U.S.C. § 103, the examiner bears the initial burden of presenting a *prima facie* case of obviousness. . . . "A *prima facie* case of obviousness is established when the teaching from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art.". . . If the examiner fails to establish a *prima facie* case, the rejection is improper and will be overturned. (Emphasis added.) 9 F.3d at 1532, 28 U.S.P.Q. 2d at 1956.

Regarding Claim 1, Claim 1 recites the following claim feature, which is neither taught nor suggested by either Rahman, Milburn or the references of record:

> an execution unit coupled to said storage area to operate on data elements in said data operand containing a portion of a user specified starting address to invalidate data in a predetermined portion of the plurality of cache lines beginning at the user specified starting address in response to receiving a single instruction of a processor instruction set. (Emphasis added.)

According to the Examiner, the feature listed above is taught by the combination of Rahman and Milburn. Applicants respectfully disagree with the Examiner's contention based on careful review of Rahman as well as Milburn.

According to the Examiner:

> Rahman shows user-specified starting address (e.g., col. 3, lines 25-35 or Abstract). In other words, based on the citation above, Rahman teaches the software routines or instructions in microcode written by a user who specified the start address to compare to the tag address. (*See* Final Office Action mailed May 5, 2004, pg. 8.)

Applicants respectfully disagree with the Examiner's contention. Specifically, as indicated by the cited passage:

> The start and end address values of the external memory device would be fetched and compared through software routines with the tag address values.

Applicants respectfully submit that the fetching of start and end address values of the external memory device do not teach or suggest a user-specified starting address, as recited by Claim 1. In other words, the start address within Rahman is based on the address range available for the external memory device according to a configuration of the external memory card. Hence, the Examiner's contention that Rahman teaches software routines or instructions in microcode written by a user who specified the starting address to the compare tag is contrary to the explicit teachings of Rahman.

Applicants respectfully submit that the user cannot specify the address ranges within an external memory device, as such parameters are set according to the manufacturing specifications of the external memory device. In other words, the user does not specify the start address to compare to the tag address, as contended by the Examiner. The start address is based on the configuration of the external memory card according to the memory capacity of the external memory card.

Conversely, Claim 1 recites a user specified starting address, which is contained in an operand of the single instruction of a processor instruction set. By way of contrast, any starting address as taught within Rahman is based on the addresses available in the external memory device. (*See* col. 3, line 36.) Consequently, Applicants submit that the user specified starting address, as recited by Claim 1, is neither taught nor suggested by the lower start address register and upper end address register, as taught by Rahman, since such registers are populated according to the available addresses in the external memory device without any user involvement.

By way of contrast, Claim 1 recites invalidating of data in a predetermined cache memory portion. Applicants respectfully submit that the predetermined portion feature recited by Claim 1 enables the use of a single instruction, since only the start address will vary between such instructions. Conversely, invalidating within Rahman is not based on a predetermined portion. The invalidated portion in Rahman will vary based on the start and end addresses of the external memory, requiring a plurality of tag address comparisons for the range defined by the start and end addresses. Applicants respectfully submit that one skilled in the art would not create a single instruction to invalidate cache contents according to the varying address ranges defined by system resources, such as an external memory.

Moreover, Claim 1 recites that the invalidating is performed in response to receiving a single instruction of a processor instruction set. Conversely Rahman performs its invalidation and

flushing in response to detected removal of the external memory. Consequently, Applicants submit that the invalidating of the cache lines of a cache memory having data from an external memory, as taught by Rahman, is not performed in response to a single instruction of a processor instruction set, as recited by Claim 1.

The Examiner recognizes Rahman's failure to teach a single processor instruction and as a result, cites Milburn. According to the Examiner:

> Milburn shows providing a single instruction with an operation code and address values in its operand (e.g., col. 9, lines 1-10; col. 10, lines 10-15; and col. 11, lines 1-20) are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a single instruction with an operation code and address values in its operand to Rahman's system because it would allow an instruction to influence multiple lines in a cache, invalidating an entire cache range, thereby reducing overall operation times. (Office Action, pg. 4.)

According to the Examiner, the concept and advantages of providing a single instruction with an operation code and address values in its operand are well known and expected in the art. Assuming, *arguendo*, that this proposition is true, the techniques described by Rahman are performed by the computer system in response to the computer system detection of removal, modification or disabling of system resources. As a result, Applicants submit that one skilled in the art would not perform the selective invalidating using a single instruction of the processor instruction set, since the techniques or instructions to perform such activity are solely performed at the direction of a computer system.

In other words, the techniques described by Rahman are performed without the knowledge of the user and therefore do not need to be made available to the user in the form of a single instruction from the processor instruction set. Accordingly, Applicants submit that one skilled in the art would not perform the selective invalidating of the cache memory of Rahman by providing a single instruction to a user, as recited by Claim 1.

Nevertheless, according to the Examiner:

> It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a single instruction with an operation code and address values in its operand to Rahman's system because it would allow an instruction to influence multiple lines in a cache, invalidating an entire cache range, thereby reducing overall operations times. (*See* Office Action, pg. 4.)

However, Claim 1 does not recite the invalidation of entire cache range, but conversely is directed toward the invalidation of a predetermined portion of cache lines beginning at a user-specified starting address. As indicated above, the predetermined portion recited by Claim 1 enables the use of a single instruction since the predetermined portion will be the same for

subsequent instructions, but will only vary according to where the predetermined portion begins, as dictated by the user-specified starting address.

Conversely, the invalidation taught by Rahman is based on an address range as defined by a start address and end address of an external memory device. Hence, Applicants respectfully submit that the modification of Rahman in view of Milburn fails to teach or suggest each of the claim features of Claim 1. In addition, since the cache line invalidation, as taught by Rahman, is strictly performed as directed by the computer system in response to computer system detection of the removal modification or disabling of system resources, Applicants respectfully submit that one skilled in the art would not be motivated by the skill in the art to include such activity within a single instruction of the processor instruction set.

Applicants respectfully submit that one skilled in the art would not be motivated to perform the modifications suggested by the Examiner since the varying address range for invalidation, as taught by Rahman, will vary according to the various system resources, such as external memory, as taught by Rahman, thereby requiring multiple comparisons and instructions to prohibit flush of the entire cache memory. Hence, Applicants respectfully submit that the Examiner's rejection of Claim 1 is based on hindsight.

Yet, it is well established that obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent the teaching or suggestion supporting such combination. ACS Hospice, Inc. v. Montefiore Hosp, 732 F.2d 1572, 1577, 221 USPQ 929, 939 (Fed. Cir. 1984) Also, one cannot find obviousness through hindsight to construct a claimed invention from elements of the prior art. In re Warner, 379 F.2d 1011, 1016, 154 USPQ 173, 177 (C.C.P.A. 1967.)

As recited by Claim 1, the single instruction, which causes data invalidation in a predetermined portion of the plurality of cache lines beginning at the user specified starting address, in response to receiving a single instruction of a processor instruction set, is not taught nor suggested by either Rahman, Milburn or the references of record. Consequently, Applicants respectfully submit that the Examiner has failed to establish a *prima facie* rejection of Claim 1 as obvious over Rahman in view of Milburn. *Id.* Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 1.

Regarding Claims 4-6, Claims 4-6 depend from Claim 1 and therefore include the patentable claim features of Claim 1, as described above. Therefore, Claims 4-6, for at least the reasons described above, are patentable over the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 4–6.

Regarding Claim 7, Claim 7 includes analogous claim features to Claim 1, as described above. Specifically, Claim 7, as amended, includes the following claim features, which are neither taught nor suggested by Rahman, Milburn or the references of record:

> an execution unit coupled to said first storage area, said second storage area, and said cache memory, said execution unit to operate on the portion of a user specified address in said data operand to copy data from a predetermined portion of the plurality of cache lines beginning at the user specified starting address in the cache memory to the first storage area, in response to receiving a single instruction of a processor instruction set. (Emphasis added.)

As indicated above, the teachings of Rahman are limited to invalidate a varying range of the contents of cache memory according to a start and end address of a system resource upon computer system detection of the removal, modification or disabling of the system resource. Applicants respectfully submit that Rahman and Milburn are devoid of any teaching regarding copying data from a predetermined portion of the plurality of cache lines beginning at the user specified starting address, as recited by Claim 7.

Accordingly, Applicants submit that the Examiner also fails to establish a *prima facie* rejection of Claim 7 as obvious under §103(a) over Rahman in view of Milburn. Consequently, Applicants respectfully request the Examiner reconsider and withdraw the §103(a) rejection of Claim 7.

Regarding Claims 8-12, Claims 8-12 depend from Claim 7 and therefore include the patentable claim features of Claim 7, as described above. Accordingly, Claims 8-12, for at least the reasons described above, are also patentable over the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 8-12.

Regarding Claim 38, Claim 38 includes the following claim feature, which is neither taught nor suggested by either Rahman, Milburn or the references of record:

> an execution unit coupled to said storage area to operate on data elements in said data operand identifying a user-definable linear or physical address identifying a predetermined portion of the plurality of cache lines to invalidate data in the predetermined portion of the plurality of cache lines in response to receiving a single cache control instruction of a processor instruction set, the single cache control instruction including a reference to the data operand.

As indicated above, both Rahman and Milburn fail to teach or suggest a user specified starting address within which to invalidate cache memory data. As indicated above, the area in which cache memory is invalidated is based on the address range available of an external memory card. Conversely, cache line invalidation, as recited by Claim 38, is performed within a predetermined portion beginning at a user-specified starting address. Furthermore, neither

Rahman, Milburn nor the references of record teach invalidation performed in response to a single decoded instruction.

Rahman does not describe a predetermined area in which invalidating is performed. The area in which invalidating is performed within Rahman is based on the address range or memory capacity of the external memory device. Hence, a single instruction cannot perform the cache range invalidation as taught by Rahman since a cache invalidation instruction is issued for each cache line with a tag falling within the address range. Applicants submit that one skilled in the art would not modify Rahman to implement invalidating of a predetermined portion of the cache memory in response to a single processor instruction set instruction since Rahman teaches invalidation of a varying cache line range by comparing each cache line tag with the range and invalidating cache lines having a tag within the range.

Consequently, Applicants submit that the Examiner cannot establish a *prima facie* rejection of Claim 38 over Rahman in view of Milburn since the combination of references fails to teach a user-definable linear or physical address identifying a portion of the plurality of cache lines to invalidate in response to a single cache control instruction, as recited by Claim 38. *Id.* Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 38.

Regarding Claims 39-41, Claims 39-41 depend from Claim 38 and therefore include the patentable claim features of Claim 38, as described above. Accordingly, Claims 39-41, for at least the reasons described above, are also patentable over the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 39-41.

Regarding Claim 42, Claim 42 includes the following claim feature, which is neither taught nor suggested by either Rahman, Milburn or the references of record:

> read a portion of an address located in a register specified in the decoded instruction to obtain a user specified starting address of a predetermined area of a cache memory on which the instruction will be performed; and invalidate in the predetermined area of cache memory. (Emphasis added.)

As indicated above, the teachings of Rahman are limited to invalidate a varying range of the contents of cache memory according to a start and end address of a system resource upon computer system detection of the removal, modification or disabling of the system resource. Applicants respectfully submit that Rahman and Milburn are devoid of any teaching regarding copying data from a predetermined portion of the plurality of cache lines beginning at the user specified starting address, as recited by Claim 42.

Accordingly, for at least the reasons described above, Applicants respectfully submit that the Examiner has failed to establish and cannot establish a *prima facie* rejection of Claim 42 since

case law clearly requires that the combination of references must teach or suggest each and every claim limitation, as required by Claim 42. *Id.* Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 42.

Regarding Claims 43-45, Claims 43-45 depend from Claim 42 and therefore include the patentable claims features of Claim 42, as described above. Accordingly, Claims 43-45, for at least the reasons described above, are patentable over the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 43–45.

Regarding Claim 46, Claim 46 includes the following claim feature, which is neither taught nor suggested by Rahman, Milburn or the references of record:

> a circuit coupled to said decoder, said circuit in response to a single decoded instruction of a processor instruction set being configured to: read a portion of an address located in a register specified in the decoded instruction to obtain a user specified starting address of a predetermined area of a cache memory on which the instruction will be performed. (Emphasis added.)

As indicated above, the teachings of Rahman are limited to invalidate a varying range of the contents of cache memory according to a start and end address of a system resource upon computer system detection of the removal, modification or disabling of the system resource. Applicants respectfully submit that Rahman and Milburn are devoid of any teaching regarding copying data from a predetermined portion of the plurality of cache lines beginning at the user specified starting address, as recited by Claim 46.

Accordingly, for at least the reasons described above, Applicants submit that the Examiner cannot establish a *prima facie* rejection of Claim 46 under 35 U.S.C. §103(a) over Rahman in view of Milburn since the combination of references of fails to teach or suggest every claim feature of Claim 46, as described above. *Id.* Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 46.

Regarding Claims 47-50, Claims 47-50 depend from Claim 46 and therefore include the patentable claim features of Claim 46. Accordingly, for at least the reasons described above, Claims 47-50 are patentable over the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 47-50.

Regarding Claims 51 and 62, Claims 51 and 62 include the following claim features, which are neither taught nor suggested by the references of record:

> in response to said decoding of the single instruction, obtaining a portion of a user specified starting address of a predetermined area of a cache memory on which the single instruction will be performed by reading a portion of an address contained in a storage location specified in the decoded instruction. (Emphasis added.)

As indicated above, the starting address referred to within Rahman refers to the start address of an available memory range or capacity of an external memory device. As indicated, the capacity and address range of the external memory device may not be modified by a user and is therefore not user specified, as required by Claim 51. Furthermore, neither Rahman nor Milburn teach the invalidating of data within the predetermined portion of memory in response to a single instruction.

As indicated, the invalidating, as described by Rahman, is performed internally within the computer in response to modification, disabling or removal of system resources and specifically, the external memory device. Moreover, Rahman does not describe a predetermined area in which invalidating is performed. The area in which invalidating is performed within Rahman is based on the address range or memory capacity of the external memory device. Hence, a single instruction cannot perform the cache range invalidation as taught by Rahman since a cache invalidation instruction is issued for each cache line with a tag falling within the address range.

Accordingly, for at least the reasons described above, Applicants respectfully submit that the Examiner cannot establish a *prima facie* rejection of Claims 51 and 62 under 35 U.S.C. §103(a) as obvious over Rahman in view of Milburn since the combination of references fails to teach or suggest each and every claim limitation of Claims 51 and 62. *Id.* Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 51 and 62.

Regarding Claims 52-55, Claims 52-55 depend from Claim 51 and therefore include the patentable claim features of Claim 51, as described above. Accordingly, Claims 52-55, for at least the reasons described above, are also patentable over the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 52-55.

Regarding Claims 56 and 63, Claims 56 and 63 include the following claim feature, which is neither taught nor suggested by the references of record:

> in response to said decoding the single instruction, obtaining a portion of a user specified starting address of a predetermined area of a cache memory on which the single instruction will be performed by reading a portion of an address contained in a storage location specified in the decoded instruction. (Emphasis added.)

As indicated above, the teachings of Rahman are limited to invalidate a varying range of the contents of cache memory according to a start and end address of a system resource upon computer system detection of the removal, modification or disabling of the system resource. Applicants respectfully submit that Rahman and Milburn are devoid of any teaching regarding copying data from a predetermined portion of the plurality of cache lines beginning at the user specified starting address, as recited by Claims 56 and 63.

Accordingly, for at least the reasons described above, Applicants respectfully submit that the Examiner cannot establish a *prima facie* rejection of Claims 56 and 63 under 35 U.S.C. §103(a) as obvious over Rahman in view of Milburn since the combination of references fail to teach the claim features of Claims 56 and 63, as described above. *Id.* Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 56 and 63.

Regarding Claims 57-61, Claims 57-61 depend from Claim 56 and therefore include the patentable claim features of Claim 56, as described above. Accordingly, for at least the reasons described above, Claims 57-61 are also patentable over the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 57-61.

Regarding Claim 64, Claim 64 depends from Claim 63 and therefore includes the patentable claim features of Claim 63. Accordingly, Claim 64, for at least the reasons described above, is also patentable over the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 64.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending (1) are in proper form, (2) are neither obvious nor anticipated by the relied upon art of record, and (3) are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,
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Dated: June 28, 2004

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. 1450, Alexandria, VA 22313-1450 on June 28, 2004

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Marilyn Bass June 28, 2004